REMARKS/ARGUMENTS

Claims 2, 4, 9, 11, 16, and 18-26 are amended. Claims 1, 8, and 15 are canceled without prejudice and without disclaimer. No new claims are added. Thus, after entry of this amendment, claims 2-7, 9-14, and 16-26 will be pending. Reconsideration of the pending rejected claims is respectfully requested.

Objection to Drawings

The drawings are objected to under 37 CFR 1.83(a) for not showing every feature of the invention specified in the claims. Regarding claims 22, 24 and 26, it is asserted that the recitation of where the input register has "... an output coupled to an input of the multiplexer" is not shown.

In FIG. 4B, the output Q of input register 455 is coupled to an input of AND gate 475, which has an output coupled to an input of multiplexer 460. Thus, output Q of the input register 455 is coupled to an input of the multiplexer 460 via AND gate 475. Accordingly, FIG. 4B does show this feature of the invention specified in claims 22, 24, and 26. For at least this reason, Applicants respectfully request withdrawal of these objections.

Rejections under 35 U.S.C. § 112, written description

Claims 22, 24 and 26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The Office Action asserts that the original specification does not connect "the input register output directly back to an input of the multiplexer." *See* Office Action, page 4.

Claim 22, 24, and 26 recite "*the input register having ... an output coupled to an input of the multiplexer.*" Note that claim 22 recites "coupled to" and not "directly connected." Thus, as described above, at least FIG. 4B does support this claim limitation. For at least this reason, Applicants respectfully request withdrawal of these rejections..

Rejections under 35 U.S.C. § 112, Herron in view of Tseng

Claims 21, 23 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herron et al., (herein Herron), U.S. Patent No. 6996758 as applied to claims 1, 8 and 15 above, and further in view of Tseng, U.S. Patent Application Publication No. 2004/0081208.

Claim 21 is allowable over the cited references, either alone or in combination, as those references fail to teach or suggest all the elements of claim 21. For example, claim 21 recites:

> *the input register having an input coupled to an output of a multiplexer and an output coupled to a first input of a logic gate, where a select input for the multiplexer is coupled to a second input of the logic gate and an output of the logic gate is coupled to an input of the IP core.*

Tseng is directed to a circuit for the control and observation of a scan chain to monitor I/O of scan cells. *See Tseng*, paragraph 6. The monitoring may be done with a multiplexer (e.g. 24) after a group of scan cells (e.g. groups 21 of scan cells 211-213). *Id.*, FIG. 2 and paragraph 21. The monitoring may also be done with control gates 31, 32, which each receive different enable signals EN_1 and EN_2 respectively. *Id.*, FIG.3 and paragraph 23. In one embodiment, control gate 31 is an AND gate 41; and in another embodiment, control gate 31 is a multiplexer 44. *Id.*, FIGS. 4A and 4D. Thus, either one may be used for a control gate, but not both. Tseng provides no mention of the enable signals for multiplexer 44 and AND gate 41 being used in conjunction with each other in the same control gate 31 or between control gates 31 and 32..

The Office Action seems to combine the separate embodiments of FIGS. 4A and 4D to obtain the select input of multiplexer 44 to also be used for AND gate 41. Contrary to this assertion, either one may be used as control gate 31, but they are not both used within a control gate as explained above. Thus, Tseng does not describe using the EN_1 signal going into multiplexer 44 also going into AND gate 41.

Additionally, even if multiplexer 44 was used for control gate 31 and AND gate 41 was used for control gate 32, different enable signals would be used. Note FIG. 3 explicitly shows different enable signals EN_1 and EN_2 for different control gates. Accordingly, the

combination of the control gate 31 of Tseng with the latch shift register 2804 of Herron does not teach or suggest "*where a select input for the multiplexer is coupled to a second input of the logic gate,*" as recited in claim 21.

For at least the reasons stated above, Applicant submits that claim 21 and its dependent claims 2-7 and 22 are allowable over the cited references. Applicants submit that claim 23 and independent claim 25 should be allowable for at least this same rationale. Claims 16-20 and 26 depend from claim 25 and thus derive patentability at least therefrom.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

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